REMARKS

This communication is in response to the first Office Action dated October 7, 2004. In that Office Action, the Examiner rejected all the claims as either being obvious in view of U.S. Patent No. 5,986,939 to Yamada. The Examiner also rejected the claims under the doctrine of double patenting based upon U.S. Patent No. 6,777,757 to Peng et al. In response, Claims 5-6 and 18-10 have been canceled. Also, a Terminal Disclaimer executed by the attorney of record is submitted herewith.

Turning to the rejection of the claims based upon the Yamada patent, Applicant notes that the Yamada patent teachers a conventional floating gate flash memory structure. As seen in the Yamada reference, a floating gate (FG) is present between the control gate (CG) and the underlying substrate. Applicant has amended the independent Claims 1, 7 and 14 to indicate that the "gate, gate dielectric, and substrate form a stack without any intervening conductive material". This limitation is not fairly shown in the Yamada reference.

Moreover, the claims of the present invention have been amended to indicate that there is a programmed doped region formed in the substrate when the memory cell has been programmed. The Examiner cites column 1, lines 48-58, as indicating that a programmed doped region is formed in the substrate after programming. To the contrary, the cited passage merely indicates that when the flash memory of the Yamada reference is erased, the charge stored on the floating gate is dissipated out through the drain. Thus, lines 54-55 state "in this condition, the electrons in the floating gate FG are extracted toward the drain D by a FN (Fowler-Nordheim) tunnel current." This does not indicate that a doped region is formed within the substrate. Indeed, conventional flash memory operates by simply tunneling the current from the floating gate out through the drain as indicated in the Yamada reference. There is no indication that a programmed doped region is formed within the substrate.

Under these circumstances, the Examiner's rejection of the claims as amended is inappropriate. Yamada is a flash memory device that uses a floating gate. Further, Yamada does not teach the formation of a programmed doped region in the substrate during programming. For these reasons, the claimed invention as amended is now in condition for allowance.

In view of the above amendment, applicant believes the pending application is in condition for allowance. Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 50-0665, under Order No. 384848005US2 from which the undersigned is authorized to draw.

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12/22/04

Respectfully submitted,

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